CLAIMS

1. A method for synchronizing a transmitter and a receiver, comprising the steps of:

generating, by the transmitter, phase difference information indicating a phase difference between an internal clock and an external clock;

transmitting, by the transmitter, the phase difference information to the receiver; and

generating, by the receiver, a clock signal dependent on the transmitted phase difference information.

2. The method according to claim 1, wherein the internal clock and the external clock are frequency-divided clocks within the transmitter to the same frequency, the method further comprising the step of converting the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

3. The method according to claim 2, further comprising the step of applying pulses of the frequency-divided clocks to start and stop inputs of a counter which generates the numerical value to be transmitted to the receiver.

4. The method according to claim 1, further comprising the step of transmitting the phase difference information to the receiver in the form of multicast packets.

5. The method according to claim 1, wherein the internal clock is a symbol clock of 80 MHz or 89.6 MHz, and the external clock is an external clock reference of 2.048 MHz or 1.544 MHz.

6. The method according to claim 1, further comprising the steps of:

generating, by the receiver, an internal clock or recovering the internal clock of the transmitter from information received from the transmitter;

frequency-dividing, by the receiver, the internal clock; and

adjusting, by the receiver, the phase of the frequency-divided clock based on the received phase difference information.

7. The method according to claim 6, further comprising the step of multiplying, by the receiver, the frequency of the adjusted frequency-divided clock for generating an external clock.

8. The method according to claim 7, comprising the step of including, by the receiver, a clock generator stage for generating the external clock, the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibiting the first counter from further counting when reaching a preset value.

9. The method according to claim 6, further comprising the steps of:

storing, by the receiver, at least two successive values of the phase difference information received from the transmitter;

detecting, by the receiver, a difference between the successive values of phase difference information; and

selecting, by the receiver, depending on the difference between the successive values of phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

10. The method according to claim 6, further comprising the steps of:

storing, by the receiver, at least two successive values of the phase difference information received from the transmitter;

detecting, by the receiver, a difference between the successive values of the phase difference information; and

suppressing, by the receiver, depending on the difference between the

successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

11. A system for synchronizing a transmitter and a receiver, the system comprises:

a transmitter comprising a phase difference information generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock, and transmitting means for transmitting the phase difference information to the receiver; and

a receiver comprising a clock generator means for generating a clock signal dependent on the transmitted phase difference information.

12. The system according to claim 11, wherein the transmitter further comprises:

a frequency divider means for frequency dividing the internal clock and the external clock to the same frequency; and

a converting means for converting the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

13. The system according to claim 12, wherein the converting means comprises a counter which generates the numerical value to be transmitted to the receiver, the counter having start and stop inputs to which pulses of the frequency-divided clocks are applicable.

14. The system according to claim 11, wherein the phase difference information is transmitted to the receiver in the form of multicast packets.

15. The system according to claim 11, wherein the internal clock is a symbol clock of 80 MHz or 89.6 MHz, and the external clock is an external clock reference of 2.048 MHz or 1.544 MHz.

16. The system according to claim 11, wherein the receiver further comprises:

a means for generating an internal clock, or for recovering the internal clock of the transmitter from information received from the transmitter;

a frequency-dividing means for frequency-dividing the internal clock; and

an adjusting means for adjusting the phase of the frequency-divided clock based on the received phase difference information.

17. The system according to claim 16, wherein the receiver further comprises a multiplying means for multiplying the frequency of the adjusted frequency-divided clock for generating an external clock.

18. The system according to claim 17, wherein the receiver further comprises a clock generator stage for generating an external clock, wherein the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibiting the first counter from further counting when the first counter reaches a preset value.

19. The system according to claim 16, wherein the receiver further comprises:

storages for storing at least two successive values of the phase difference information received from the transmitter;

a detector means for detecting a difference between the successive values of the phase difference information; and

a selector means for selecting, depending on the difference between the successive values of the phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

20. The system according to claim 16, wherein the receiver further comprises:

storages for storing at least two successive values of the phase difference information received from the transmitter;

a detector means for detecting a difference between the successive values of the phase difference information; and

a suppressing means for suppressing, depending on the difference between the successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

21. A transmitter used in a system for synchronizing a transmitter and a receiver, wherein the receiver comprises a clock generator means for generating a clock signal dependent on the transmitted phase difference information, the transmitter comprising:

a phase difference generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock; and

a transmitting means for transmitting the phase difference information to a receiver.

22. The transmitter according to claim 21, comprising:

a frequency divider means for frequency dividing the internal clock and the external clock to the same frequency; and

a converting means for converting the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

23. The transmitter according to claim 22, wherein the converting means comprises a counter which generates the numerical value to be transmitted to the receiver, the counter having start and stop inputs to which pulses of the frequency-divided clocks are applicable.

24. The transmitter according to claim 21, comprising a packet generator means for transmitting the phase difference information to the receiver in the form of multicast packets.

25. The transmitter according to claim 21, wherein the internal clock is a symbol clock of 80 MHz or 89.6 MHz, and the external clock is an external clock reference of 2.048 MHz or 1.544 MHz.

26. A receiver used in a system for synchronizing a transmitter and a receiver, wherein the transmitter comprises a phase difference generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock and means for transmitting the phase difference information to the receiver, the receiver comprising:

a clock generator means for generating a clock signal dependent on a phase difference information transmitted from a transmitter.

27. The receiver according to claim 26, further comprising:

means for generating an internal clock, or for recovering the internal clock of the transmitter from information received from the transmitter;

a frequency-dividing means for frequency-dividing the internal clock; and

an adjusting means for adjusting the phase of the frequency-divided clock based on the received phase difference information.

28. The receiver according to claim 26, further comprising a multiplying means for multiplying the frequency of the adjusted frequency-divided clock for generating an external clock.

29. The receiver according to claim 26, further comprising a clock generator stage for generating an external clock, the clock generator stage comprises a first counter

for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibits the first counter from further counting when the first counter reaches a preset value.

30. The receiver according to claim 26, comprising:

storages for storing at least two successive values of the phase difference information received from the transmitter;

a detector means for detecting a difference between the successive values of the phase difference information; and

a selector means for selecting, depending on the difference between the successive values of the phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

31. The receiver according to claim 26, comprising:

storages for storing at least two successive values of the phase difference information received from the transmitter;

a detector means for detecting a difference between the successive values of the phase difference information; and

a suppressing means for suppressing, depending on the difference between the successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

32. A method for synchronizing a transmitter and a receiver wherein the receiver generates a clock signal dependent on a transmitted phase difference information, the method comprising the steps of:

generating, by a transmitter, phase difference information indicating a phase difference between an internal clock and an external clock; and

transmitting, by the transmitter, the phase difference information to the receiver.

33. A method for synchronizing a transmitter and a receiver wherein the transmitter generates phase difference information indicating a phase difference between an internal clock and an external clock, the method comprising the step of:

generating, by the receiver, a clock signal dependent on a transmitted phase difference information indicating a phase difference between the internal and the external clock of the transmitter, the phase difference information being received from the transmitter.